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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,138	SAHA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-20 and 24-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-20 and 24-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/21/2009.

2. Claims 1-7, 10-20 and 24-34 are pending in this application. Claims 1, 3, 5, 16, 27 and 31 are independent claims. In Amendment, claims 8-9 and 21-23 are cancelled and claims 24-34 are added. This Office Action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claims 24-34 must be shown or the feature(s) canceled from the claim(s), particularly the limitations of independent claims 27 and 31 wherein the part of computing remaining butterfly stages...of the iteration of the loop. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 24-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claims 24-26, the limitations "the multiprocessor system to perform spectral analysis; to filter the digital signal in frequency domain; and to perform polyphase transformation" are briefly mentioned in the background of the invention, but these limitations have never fully addressed in the summary or detail of the invention of the original specification in a way that would be able to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention within the context of the claims.

Re claims 27-34, the limitations within these claims are not fully described in the original specification in a way to enable one skilled in the art to which it pertains, or with

which it is most nearly connected, to make and/or use the invention, in particular the limitations of "computing remaining butterfly stages of....of an iteration of the loop" since at most the Figures 2-3 merely suggest independent or no dependency in the first couple stages only.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 5-6 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 5, the limitation "computer-readable memory medium" is unclear since the specification does not fully address the definition or type of the computer-readable memory medium. For examination purposes, the examiner considers the "computer-readable memory medium" as the tangible medium as RAM, ROM, hard drive, and CD-ROM. Claim 16 has similar rejection.

Thus, claims 6 and 17-20 are also rejected for being dependent on the rejected base claims 5 and 16 respectively.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1-4, 7, 10-15 and 24-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-4, 7, 10-15 and 24-34 cite a method and system for performing a/an FFT/IFFT in accordance with a predetermined mathematical algorithm. However, claims 1-4, 7, 10-15 and 24-34 merely disclose steps/components for performing FFT/IFFT without disclosing a practical/physical application. Further, the method claims 1-2, 7, 10-11 and 24-30 fail to tie to specific machine or apparatus. Even though, these claims mention multiprocessor but they did not provide sufficient structure of the multiprocessor in order to be specific machine or apparatus. Therefore, claims 1-4, 7, 10-15 and 24-34 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-7, 10-20 and 24-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abel et al. (U.S. 5,991,787) in view of Jaber (U.S. 6,792,441).

Re claim 1, Abel et al. disclose in Figures 1-14 method of processing a digital signal under control of instructions executing on a multiprocessor computing system by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11

discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal in a memory (e.g. Figures 15-16 and col. 13 lines 10-45).

Abel et al. fail to disclose in Figures 1-14 a linear scalable method of the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, Jaber discloses in Figures 8-9 a linear scalable method (e.g. by means of independent and distribute among processors as seen in Figure 8) of the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract and col. 3

lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a linear scalable method of the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 2, Abel et al. fail to disclose in Figures 1-14 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor. However, Jaber discloses in Figures 8-9 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor (e.g. col. 7 lines 2-30).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required

for each specific butterfly operation assigned to the processor as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 3, it is a system claim having similar limitations of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a system claim having similar limitations of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, Abel et al. disclose in Figures 1-14 a computer-readable memory medium whose contents cause a system having a plurality of processors to perform a method of transforming a signal by computing with the plurality of processors a FFT or IFFT of the signal using a decimation in time approach, the method comprising: computing a first and second stage of logzN stages of the N- point FFT/IFFT as a single radix-4 butterfly operation (e.g. component 900 in Figure 9) while implementing the remaining (log2N-2) stages (e.g. Figures 4 and 8) using radix-2 butterfly operations (e.g. component 800 in Figure 8 wherein the component 800 utilizes radix-2 to compute the butterfly computation of IFFT), wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal in a memory (e.g. Figures 15-16 and col. 13 lines 10-45).

Abel et al. fail to disclose in Figures 1-14 a linear scalable method of the multiprocessing system for distributing the plurality of butterfly operations in each stage

of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, Jaber discloses in Figures 8-9 a linear scalable method (e.g. by means of independent and distribute among processors as seen in Figure 8) of the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a linear scalable method of the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 6, it has similar limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 7, Abel et al. further disclose in Figures 1-14 the first radix is a radix-2 radix (e.g. component 800 in Figure 8 wherein the component 800 utilizes radix-2 to compute the butterfly computation of IFFT).

Re claim 10, Abel et al. further disclose in Figures 1-14 an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT (e.g. output of Figure 4 or Figure 8).

Re claim 11, Abel et al. fail to disclose in Figures 1-14 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location. However, Jaber discloses in Figures 8-9 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location (e.g. col. 15 lines 4-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 12, it is a system claim having similar limitations of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, Abel et al. further disclose in Figures 1-14 computing a first and second stage of logzN stages of the N- point FFT/IFFT as a single radix-4 butterfly operation (e.g. component 900 in Figure 9).

Re claim 14, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises (log2N-2) stages (e.g. Figures 4 and 8).

Re claim 15, it is a system claim having similar limitations of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a computer-readable memory claim having similar limitations of claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a computer-readable memory claim having similar limitations of claim 2. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a computer-readable memory claim having similar limitations of claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 19, it is a computer-readable memory claim having similar limitations of claim 14. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 20, it is a computer-readable memory claim having similar limitations of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claims 24-26, Abel et al. fails to disclose the multiprocessor system to perform spectral analysis on the digital signal; to filter the digital signal in frequency domain; and to perform polyphase transformation. However, Jaber discloses the multiprocessor system to perform spectral analysis on the digital signal; to filter the digital signal in frequency domain; and to perform polyphase transformation (e.g. col. 1 lines 30-52).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiprocessor system to perform spectral analysis on the digital signal; to filter the digital signal in frequency domain; and to perform polyphase transformation as conceptually seen in Jaber's invention into Abel et al.'s invention because it would enable to reduce the computational burden in signal processing (e.g. col. 1 lines 44-52).

Re claim 27, Abel et al. disclose in Figures 1-14a method of transforming a digital signal (e.g. abstract and col. 1 lines 30-40), the method comprising: computing, with a multiprocessor computing system having a plurality of processor P, a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT and either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively); and storing the transformed digital signal in a memory medium e.g. Figures 15-16 and col. 13 lines 10-45).

Abel et al. fail to disclose in Figures 1-14 the multiprocessing system comprising a plurality of processors P for computing remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop. However, Jaber discloses in Figures 8-9 the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) comprising a plurality of processors P (e.g. Figure 8) for computing remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiprocessing system comprising a plurality of processors P for computing remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claims 28-29, Abel et al. fail to disclose in Figures 1-14 the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages. However, Jaber discloses in Figure 8 the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage (e.g. Figure 8 with only two processors A and B) and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages (e.g. Figure 8 with only four processors as indicated by dot ….).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages as conceptually seen in Jaber's invention into Abel et al.'s invention because it would enable to reduce the computational burden in signal processing (e.g. col. 1 lines 44-52).

Re claim 30, Abel et al. further disclose in Figures 1-14 transforming the digital signal comprises filtering the digital signal in a frequency domain (e.g. col. 1 lines 35-40).

Re claim 31 it is a system claim having similar limitations of claim 27. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 27.

Re claim 32 it is a system claim having similar limitations of claim 28. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 28.

Re claim 33 it is a system claim having similar limitations of claim 29. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Re claim 34 it is a system claim having similar limitations of claim 30. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 30.

Response to Amendment

12. The amendment filed 01/21/2009 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Re claims 27 and 31, the limitations "computing remaining butterfly stages of….of an iteration of the loop" within these claims are not fully described in the original specification which introduce new matter into the disclosure of the invention. Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

13. Applicant's arguments with respect to claims 1-7, 10-20 and 24-34 have been considered but are moot in view of the new ground(s) of rejection.

14. Applicant's arguments filed 01/21/2009 have been fully considered but they are not persuasive.

a. The applicant argues in pages 9-11 for claims rejected under 35 U.S.C. 101 that the processing a digital signal is a practical application and further the claims perform using a multiprocessor system which includes storing of the results of the process in a memory.

The examiner respectfully submits that the rejection of claims under 35 U.S.C. 101 of the last Office Action was withdrawn most grounds but still maintained two issues as (1) non-practical application and (2) the method claims do not sufficiently provide or tie to specific machine or apparatus as require. (1) merely processing signal is not practical application since it does not provide or show any practical use or tangible use of processing the signal. (2) merely mention multiprocessor system would not sufficient to place the method claims statutory since they do require to tie to specific machine or apparatus wherein general memory and processor themselves would not consider as specific machine or apparatus.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

May 11, 2009